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An Approach for Low Power CMOS Design

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Abstract
Power dissipation has emerged an important parameter in design of Low Power CMOS circuits. For this level converter and dual supply voltage assignments are used to reduce the power dissipation and propagation delay. In this paper, variable supply-voltage scheme (dual-VS scheme) for dual power supplies along with voltage level converter is presented. Also paper presents an overall comparative analysis among various methods to achieve voltage level shifter even in lower technology comparative to higher ones and help user to select the best methods for same at this technology.
***Keywords*:** Dual-V_{DD}, Dual-VS scheme, Level Converter, Level Shifter.

I. INTRODUCTION

A source of power dissipation on digital integrated circuit depends on the different states which are power dissipation due to charging and discharging of circuit nodes and capacitance (indicated by C) is known as switching power dissipation. Power dissipation during output transition due to current flowing from the supply to ground is known as short circuit power dissipation [1], [2]. Power dissipation due to leakage current which sub-threshold, gate, junction, contention currents is known as static power dissipation as shown in figures 1(a-c).

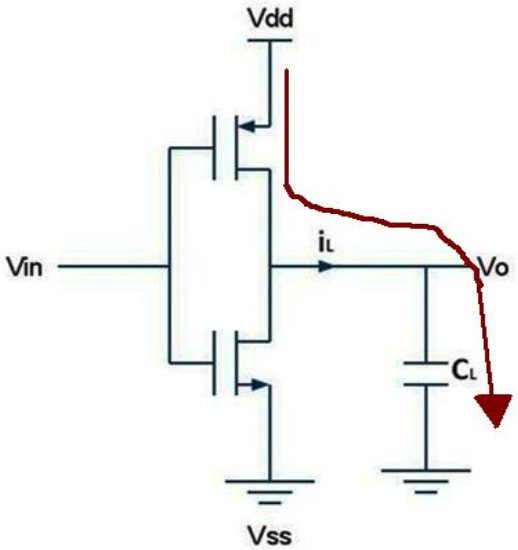


Figure 1(a). Digital Integrated Circuit CMOS Inverter

- Switching component is energy for charge parasitic capacitors (gate, diffusion, and interconnect)

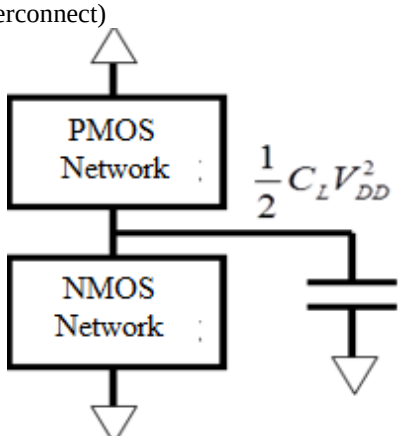


Figure 1(b) In CMOS, Output Nodes are Charged

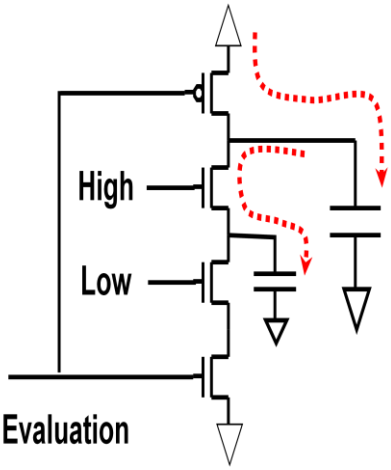


Figure 1(c) Charge Sharing or Discharged

- Short circuit component is finite rise and fall time → direct current path between V_{dd} and GND $V_{th} < V_{in} < V_{dd} < V_{tp}$ (Both NMOS and PMOS are turned on).
- Leakage component are reverse biased PN junction sub-threshold, gate, junction, contention currents as shown in below figure 1(d).
  Power dissipation optimization focuses on minimization switching activity and power at different level of design.

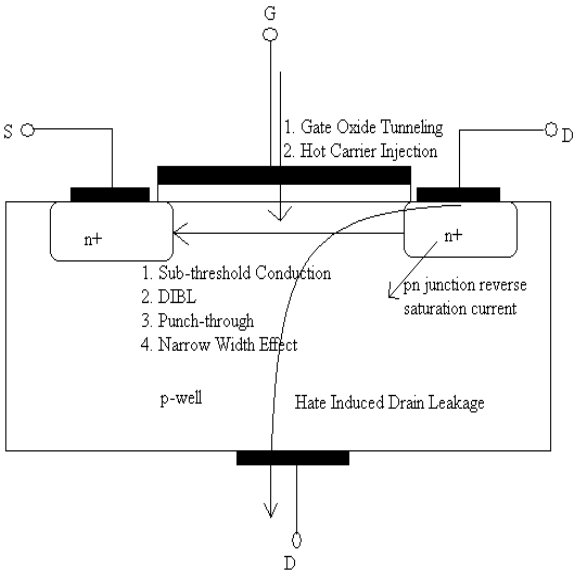


Figure 1(d) Reverse Biased PN Junction Sub-Threshold

$$P_{static} = \left(I_{sub\ threshold} + I_{gate} + I_{junction} + I_{contention}\right)V_{dd} \quad (1)$$

$$P_{dynamic} = \left(P_{switching} + P_{short\ circuit}\right) \quad (2)$$

Total power dissipation

$$P_{total} = \left(P_{static} + P_{dynamic}\right) \quad (3)$$

The presented techniques and approach come down to a fundamental set of concepts power dissipation is reduced by lowering either the supply voltage, the voltage swing, the physical capacitance, the switching activity or combination above at different design abstraction layer.

The paper is organized as follows. The operation of dual-V_{DD} design is described in next section. In Section 3, dual VS Scheme is proposed. The operation of the level converters is described in Section 4. Section 5 describes level shifter which is used to shift the level of voltages. Finally, some conclusions are provided in the last section.

II. DUAL V_{DD} DESIGN

Dual-V_{DD} design is an effective way to reduce power consumption, but the need for level conversion imposes delay and energy penalties that limit the potential gains**.** Dynamic power dissipation in CMOS circuits is proportional to the square of the supply voltage. A reduction in V_{DD} thus considerably lowers the power dissipation of the circuit. Dual-V_{DD} design is an important scheme that exploits this concept to reduce power consumption in integrated circuits [3], [4]. Since a reduction in V_{DD} degrades circuit performance, in order to maintain performance in dual-V_{DD} designs, cells along critical paths are assigned to the higher power supply (V_{DDH}) while cells along noncritical paths are assigned to the lower power supply (V_{DDL}).The dual-V_{DD} design scheme can be generalized into a dual-V_{DD} / dual-V_{TH} design scheme where the threshold voltage of the transistors may take one of two different values (we denote the lower V_{TH} by V_{THL} and the higher V_{TH} by V_{THH} [5]**.**

Most high-performance CMOS processes today offer dual threshold voltages. Level converter circuits can leverage the availability of this second V_{TH} to maintain good speed characteristics when converting from very low voltages such as those we describe in this work [6]. Transistors in the level converting circuits that we study are selectively assigned to V_{THL} or V_{THH} based on their delay criticality within the overall circuit. ECVS (and hence, these asynchronous LCs) will be most effective when the clock cycle is not highly aggressive, since the delay overhead of several such level converters per logic path is prohibitive for heavily pipelined designs like microprocessors [7].
In the next two sections asynchronous level converter and synchronous level converter are described for their performance and robustness.

2.1 Asynchronous Level Converter Design and Analysis

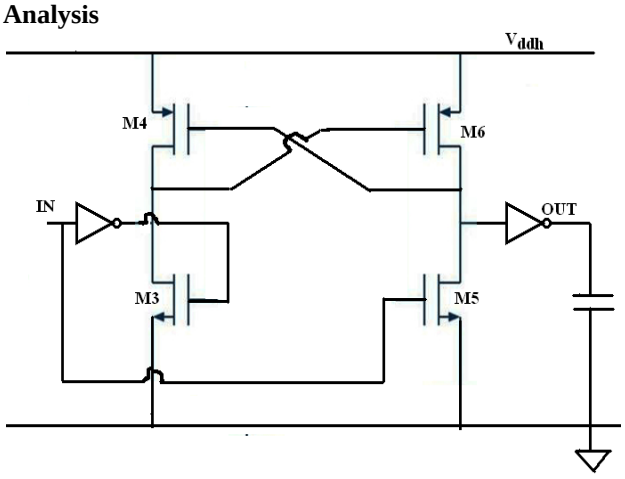


Figure 2(a). Existing and Proposed Asynchronous Level Converter Topologies. Transistor Labeled with (*) Indicate Low-V_{th} Devices

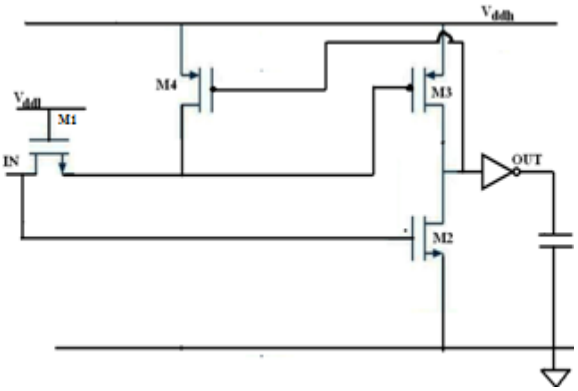


Figure 2(b). Existing and Proposed Asynchronous Level Converter Topologies. Transistor Labeled with (*) Indicate Low-V_{th} Devices

Figure 2(a) and (b) shows two level converters that have been presented previously and the new level converters that we propose, figure 2(c)–(d). Figure 2(a) shows a traditional level converter, which is a differential cascade voltage switched (DCVS) logic gate [8], [9]. Here, the input arrives at V_{ddl} and is up-converted to V_{ddh} through the cross-coupled pMOS device pair formed by transistors M4 and M6. This converter consumes significant energy due to the contention at the points of connection of the cross-coupled pair and the pull-down nMOS network formed by M3 and M5. Figure 2(b) [labeled PG] shows a level converter described in [10] that is based on a weak feedback pull-up device (M4) and nMOS pass gate (M1). The purpose of the pass gate device is to isolate the input of the pMOS M3 from the previous logic stage. The feedback device M4 can then pull-up the internal node without consequence to the prior logic that is running at V_{ddl}. This level converter consumes less energy than the DCVS level converter due to its fewer devices and reduced contention. All new level converters that we propose are based on this level converter.

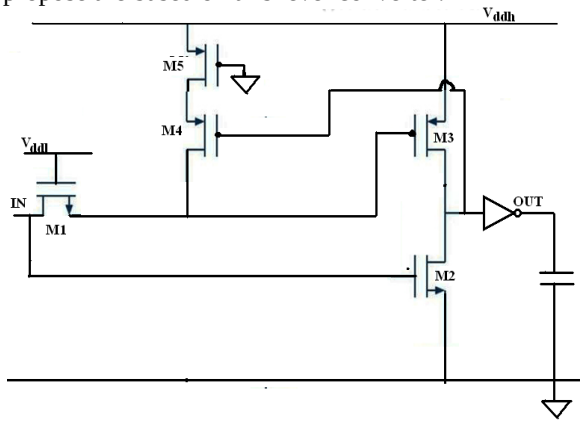


Figure 2(c). Existing and Proposed Asynchronous Level Converter Topologies.

Figure 2(c) [STR1] shows the first new level converter that we propose. As seen in the figure, the feedback device M4 (keeper) from figure 2(b) is split into two devices M4 and M5. This is a known high-performance dynamic design technique and the advantage of this change is to reduce the capacitive load (gate capacitance of the keeper device) on node N [in figure 2(c)]. When sized properly, M5 is larger than M4 (which tends to minimum width and length) thus reducing the loading on transistors M2 and M3 by the keeper. This allows M2 and M3 to be sized smaller, reducing the total energy consumption [11].

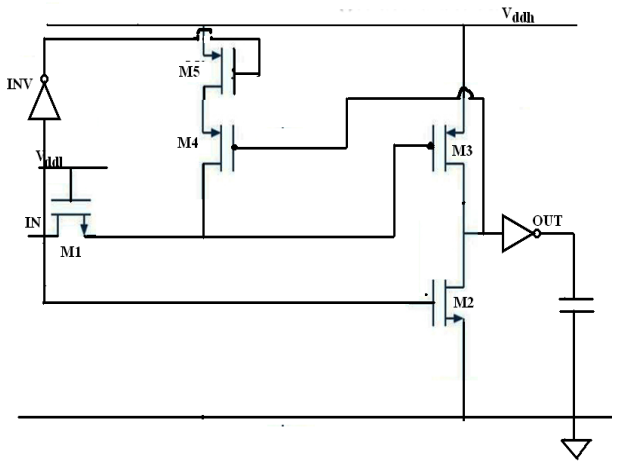


Figure 2(d). Existing and Proposed Asynchronous Level Converter Topologies. Transistor Labeled with (*) Indicate Low-V_{th} Devices

Figure 2(d) STR2, is an extension of STR1, where inverter INV (supplied by V_{DDL}) is added to drive the keeper device M5. The goal is to turn off the feedback path faster (as soon as the input starts falling) in order to speed the falling transition at the output since a falling transition at the input defines the critical path for the basic PG level conversion circuit. The addition of INV reduces the contention caused by the keeper when the input is going low as the keeper M5 is substantially weakened, though not completely turned OFF (INV which is driven by V_{DDL} Cannot completely turn OFF M5 since its source is connected to V_{DDH}).

2.2 Synchronous Level Converters

Scaling V_{DD} down in circuits reduces both dynamic power and static leakage power besides reducing the performance. To reduce power consumption without degrading performance, a dual-V_{DD} technique exploits time slacks and lowers voltage V_{DDL} for gates on non-critical paths. As shown in figure 3(a), a clustered voltage scaling (CVS), normally known as synchronous level converter, algorithm does not allow the V_{DDL} cells to feed directly into V_{ddh} cells and so level converting is implemented inside the flip-flop (LCFF). This topological limitation reduces full use of time slacks that exist in a circuit. The extended clustered voltage scaling (ECVS) in figure 3(b) eliminates this

constraint by inserting a level converter (LC) in figure 3(c) with each V_{ddl} cell feeding into a V_{ddh} cell. ECVS gives better power saving than CVS but LC adds to power and delay overheads.

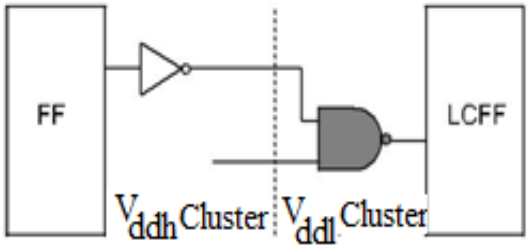


Figure 3(a) Clustered Voltage Scaling (CVS)

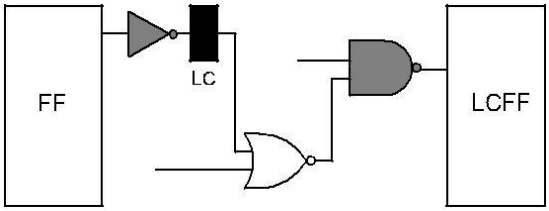


Figure 3(b) Extended Clustered Voltage Scaling (ECVS)

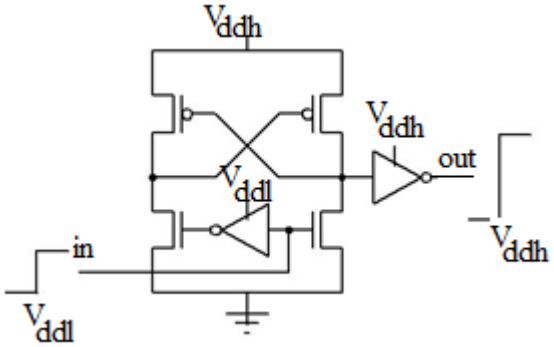


Figure 3(c) Level Converter (LC)

Without a level converter the low to high output transition delay of the second stage inverter is not affected by the input voltage swing V_{ddl} from the previous stage, because the delay of the pull-up PMOS is only dependent on its own power supply V_{DDH}. During the high to low output transition of the second inverter, the pull-down NMOS delay is affected by both the input swing V_{ddl} and the power supply V_{ddh}. Therefore, lower input swing reduces discharge current through the NMOS, which increases the pull-down delay. Because the pull-up PMOS in the inverter could not be shut off completely by the lower input swing level; severe DC current from the power supply V_{ddh} induces higher static leakage power consumption.

In next section, the dual-VS scheme is proposed. The theory of the optimal V_L is presented after that followed by Level Converter in section 4.

III. DUAL-Voltage Supply Scheme

Dual supply voltages are adaptively generated and optimally provided to internal circuits. The VS scheme for dual power supplies, namely, the dual-VS scheme, is proposed. A theory about the optimal V_L is presented, which aids designers in deciding on the optimal supply voltages.

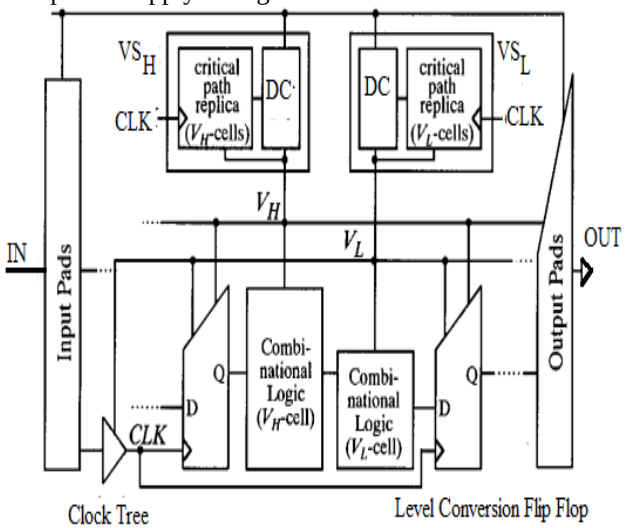


Figure 4. Dual-Supply Voltage (VS) Scheme.

The dual-VS scheme is illustrated in figure 4. There are two circuit clusters: one operating under V_H (V_H cell) and the other under V_L (V_L cell). V_H and V_L generated by an embedded power supply VS_H and VS_L, respectively. Each of them monitors circuit speed of a critical path replica under its generating voltage for an adaptive control. Both flip-flops and clock circuits are operated under V_L to reduce power dissipation. It is therefore necessary to insert level-converters between the flip-flops and the V_H cells.

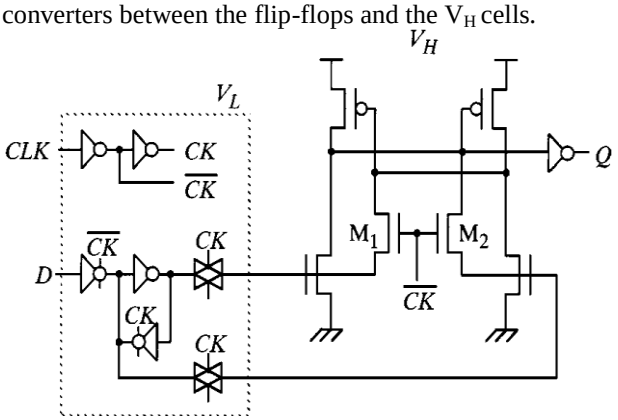


Figure 5. Level-Conversion Flip-Flop.

A circuit that functions as both the flip-flop and the level converter, the level-conversion flip-flop (LC-F/F) in figure 5, is developed [12]**.** When a clock CLK is high (V_L), n-channel transistors M_1 and M_2 are turned off, and the slave is equivalent to a conventional level-conversion circuit. At this time, the master is holding data that passes to the level-

conversion circuit. When CLK is low, M_1 and M_2 are turned on, and the slave is equivalent to a latch. At this time, the master is transparent but disconnected from the slave. Therefore, data when CLK was high are stored in the slave and output. In this way, at the rising CLK edge, V_L-swing data are captured which will be stored and converted to the V_H -swing signal for output till the next CLK edge. Power, delay, and area of LC-F/F are smaller than those of the conventional flip-flop plus level converter by 14, 41 and 26%, respectively [13], [14].

For stable control, consider two virtual critical paths, each of which is composed of only the V_H cells or the V_L cells and whose delay is equal to or a little slower than the real critical path. Now consider controlling the virtual critical paths by putting them in the replica circuits in VS_H and VS_L. The dual supplies can be controlled independently and hence stably. The critical path replicas in VS_H and VS_L are implemented by a gate chain. The number of the stages of the gate chains is designed such that delay of the two critical path replicas is equal to the cycle time at the optimal V_H and V_L. In other words, the ratio of the number of the stages of the gate chains is inversely proportional to the ratio of the gate delay at the optimal V_H and V_L. Consequently, the gate delay under V_H is proportional to the gate delay under V_L, and thus the relative delays of all the real paths are maintained. It is, therefore, guaranteed that no new critical path appears that is slower than the virtual critical path. The stability and error of this control scheme are examined through chip evaluation.

IV. LEVEL CONVERTERS

The standard feedback-based level converter (LC1) [15] is shown in figure 6.

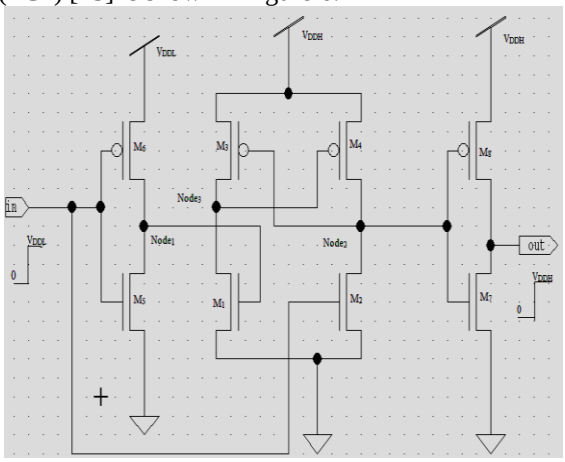


Figure 6. Standard Level Converter (LC1) presented in [13]. V_{DDL} is The Lower Supply Voltage. V_{DDH} is the Higher Supply Voltage.

M1 and M2 experience a low gate overdrive ($V_{ddl} - V_{th}$) voltage during the operation of the circuit. M1 and M2 and need to be sized larger to produce more current as compared to and, respectively, for functionality.

The circuit operates as follows. When the input is at 0 V M2 is turned off. Node1 is charged to V_{DDL}. M1 is turned on. Node3 is discharged to 0 V turning M4 on. Node2 is charged to V_{DDH} turning M3 off. The output is pulled down to 0V. When the input transitions to V_{DDL}, M2 is turned on. Node1 is discharged, turning M1 off. Node2 is discharged, turning M3 on.Node3 is charged up to V_{DDH} turning M4 off. The output transitions to V_{DDH}.

A feedback loop, isolated from the input, controls the operation of M3 and M4 during both transitions of the output. Due to the transitory contention between the pull-up and the pull-down networks and the large size of the nMOS transistors (M1 and M2), however, LC1 consumes significant short-circuit and dynamic switching power. To maintain functionality with the lower values of V_{DDL}, the sizes of M1 and M2 need to be further increased in order compensate for the gate overdrive degradation.

The load seen by the previous stage (driver circuit) is therefore increased, thereby further degrading the speed and increasing the power consumption. Tapered buffers are required to drive and at very low voltages. These tapered buffers further increase the power consumption of LC1 [16].

4.1 Multi Threshold (V_{th}) Converters

New proposed multi V_{th} employ a multi V_{th} CMOS technology in order to eliminate the static DC current the high threshold voltage pull-up network transistors in new level converter are directly driven by the low swing signals without producing a statics DC current problem. The First proposed level converter (PLC) is in the figure 7 is made by two cascaded inverter with dual V_{th} transistors.

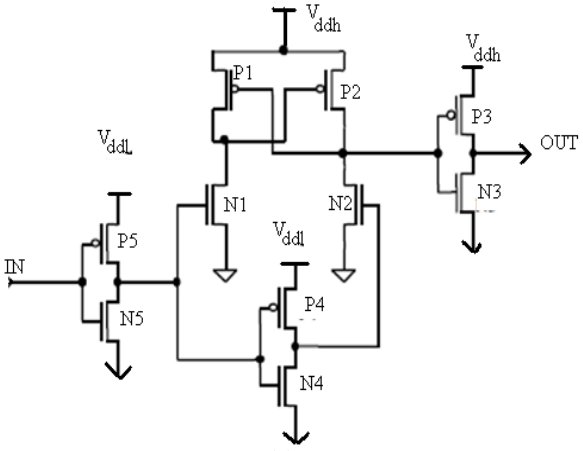
The threshold voltage of is more negative (higher $|V_{th}|$) for avoiding static dc current in the first inverter when the input is at V_{DDL}. $|V_{th}$-M2| is required to be higher than V_{DDH}- V_{DDL} for eliminating the static dc current. PC1 operates as follows. When the input is at 0 V, M2 is turned on.M1 is cutoff. Node1 is pulled up to V_{DDH}. The output is discharged to 0 V. When the input transitions to V_{DDL}, M1 is turned on. M2 is turned off since V_{GS}, M2 > V_{th}, M2. Node1 is discharged to 0 V. The output is charged to V_{ddh} [17], [18].

However, in SOC (system-on-chip) different blocks of the circuit requires different voltage level to operate perfectly and when the signal is transferred from high voltage block to low voltage block, voltage level shifter circuits play an important role as described in next section.

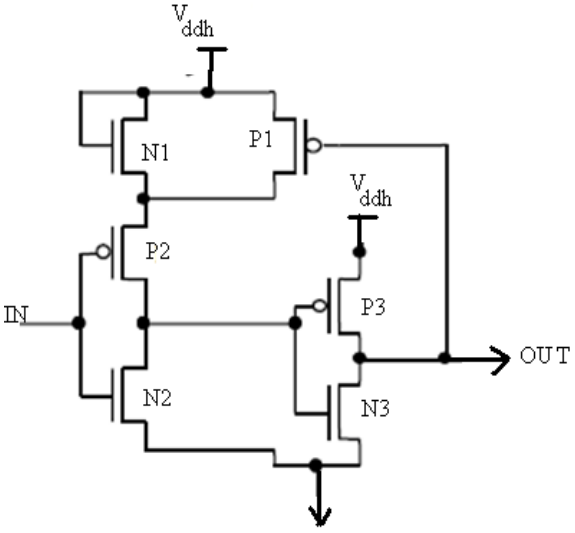
V. LEVEL SHIFTER

Level shifter is a circuit which is used to shift the level of voltages. There are two types of level shifters: a positive voltage level shifter used to transfer the voltage level from lower positive level to higher positive level and a negative voltage level shifter used to transfer the voltage from higher level to lower voltage level.

Multiple supply voltages techniques have been proposed for low power design. With the use of two different supply voltages, it is possible that a low voltage gate is made to drive a high-voltage one. This leads to the high output of the low-voltage gate cannot fully turn off the PMOS part of the high-voltage gate, so it forms a DC leakage path from the power source to ground. The DC leakage can lead to substantial power loss. To solve this problem, a level shifter is used at the interface of a low-voltage and high-voltage gates [19].



(a)



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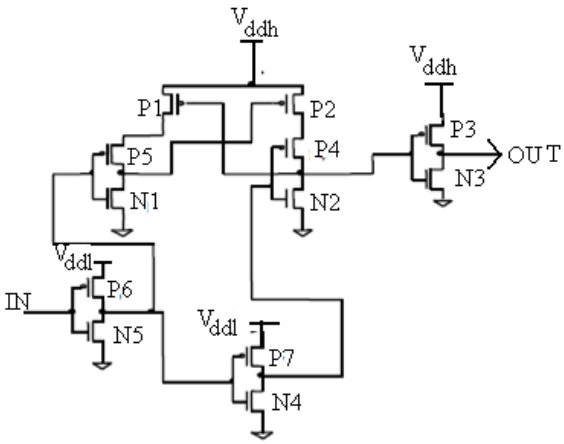

(c)

Figure 8 Level Shifter Circuits (a) Conventional (b) Single Supply (c) Contention Mitigated

The level shifter is a key circuit component in multi-voltage circuits and has important implementation. For a chip-level DVS system, level Shifters are required between core circuits and I/O circuits interface where low voltage logic signals from chip core are shifted to high voltage level at which pad Ring is working. Since the level shifter circuit consumes power and has a considerable delay, how to optimize the performance to gain low power and small delay and how to minimize the number of level shifters are important in the voltage scaling technique.

In present devices, it is required that more and more circuits can be designed on a single chip [20]. However, in Soc all the different block of the circuit required the different voltage level to operate perfectly and when the signal transfer from high voltage block to low voltage block vice-versa, here the voltage level shifter circuits play major role. If we talk about the power consumption, it is obvious that power consumed by the CMOS circuit is directly proportional to the supply voltage. Therefore, it is required that the level shifter design must be attractive in reducing power consumption, delay and area while maintaining its intended purpose [21].

With increase in operating frequency and number of level shifters in data driver's circuits, power consumption has become major performance metrics. It has been reported that stacking of two off devices reduces the sub-threshold leakage as compared to single off device [22]-[24].

VI. CONCLUSION

In this paper, dual-VS scheme is presented and level-conversion flip-flop is developed. It is found in theory, that the lower supply voltage should be set at 0.7 of the higher supply voltage to minimize chip power dissipation. This knowledge aids designers in

deciding on the optimal supply voltages, which is essential for short design time. Further we studied different level converters based on feedback in order to suppress the dc current paths in CMOS gates driven by low-swing input signals. Also various designs of voltage level shifter have been studied on the basis of output voltage, power consumed and delay.

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